



GIRIJANANDA CHOWDHURY UNIVERSITY, ASSAM

Hatkhowapara, Azara, Guwahati 781017, Assam

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course structure for Specialization in Semiconductor Technology

Semester	Theory	Practical	Course code	Credit
3rd sem	Introduction to VLSI Design		BEC23162T	3
4th sem	Digital Design with HDL	HDL Coding and Simulation (Verilog/VHDL)	BEC23203T	3
5th sem	Analog and Mixed-Signal Design		BEC23164T	3
6th sem	EDA Tools for VLSI Design	CMOS Circuit Simulation using EDA Tools	BEC23205T	3
7th sem	Elective Modules: Low-Power VLSI Design / Physical Design and Verification / VLSI Testing and Verification.		BEC23166T	3
8th sem:	Physical Design Hands-On (Cadence/Synopsys Tools) with project work		BEC23207T	3
Total credit:				18



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BEC23162T	INTRODUCTION TO VLSI DESIGN	3L:0T:0P	3 Credits
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Course Outcomes

After completing the course, students will be able to:

1. Understand Semiconductor Fundamentals
2. Analyze MOSFET Theory and Characteristics
3. Understand CMOS Technology
4. Gain Insight into VLSI Technology
5. Apply Principles of Digital and Analog Electronics
6. Understand the VLSI Design Flow
7. Familiarize with EDA Tools

Topics	No of lectures
Module 1: Basics of Semiconductor Physics	6
Introduction to Semiconductor Materials: Intrinsic and extrinsic semiconductors, Carrier concentration and mobility, Generation and recombination processes	
Energy Bands and Transport Mechanisms: Bandgap theory, Drift and diffusion currents, Continuity equation and Poisson's equation	
pn Junctions : Structure and characteristics, Junction capacitance and depletion region.	
Module 2: MOSFET Theory and Characteristics	7
MOSFET Basics: Structure and operation of nMOS and pMOS transistors, Threshold voltage ($V_{T, TT}$) and body effect	
I-V Characteristics of MOSFETs : Linear, saturation, and cut-off regions, MOS capacitance and C-V characteristics	
Second-Order Effects: Short-channel effects, Subthreshold conduction, Channel-length modulation and hot carrier effects.	
Module 3: CMOS Technology Overview	9
CMOS Technology Basics: CMOS fabrication process overview, n-well, p-well, twin-tub, and SOI technologies.	
CMOS Logic Design: CMOS inverter: DC transfer characteristics, noise margins, Design of basic gates (AND, OR, NAND, NOR) using CMOS	
CMOS Circuit Properties: Power dissipation (static and dynamic), Propagation delay and sizing.	
Advantages of CMOS Technology: Scalability, power efficiency, and integration	
Module 4: Overview of VLSI Technology	6
Introduction to VLSI and its Evolution: Historical perspective and Moore's Law, Classification of design methodologies: full-custom, semi-custom, and programmable logic	
Fabrication Steps: Wafer preparation, photolithography, ion implantation, Diffusion, etching, oxidation, and metallization.	



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Packaging and Testing: Overview of IC packaging types, Yield and reliability considerations	
Module 5: Basics of Digital and Analog Electronics	
Digital Electronics Review: Logic gates, combinational circuits, and sequential circuits, Boolean algebra, multiplexers, and flip-flops, Arithmetic circuits: adders, subtractors, and ALUs.	7
Analog Electronics Review: Amplifiers and operational amplifier basics, Filters, oscillators, and ADC/DAC converters, Basics of frequency response and bandwidth	
Module 6: VLSI System Design Flow	
Design Flow Overview: Steps in the VLSI design process: specification, RTL design, synthesis, verification, and layout	5
Front-End Design: RTL coding using HDLs (Verilog or VHDL), Functional verification using simulation tools.	
Back-End Design: Physical design: floorplanning, placement, and routing, Design rule checking (DRC) and layout versus schematic (LVS) verification	
EDA Tools: Overview of industry-standard tools (Cadence, Synopsys, Mentor Graphics)	

Reference Books and Materials

1. *Principles of CMOS VLSI Design* by Neil Weste and Kamran Eshraghian.
2. *CMOS Digital Integrated Circuits* by Sung-Mo Kang and Yusuf Leblebici.
3. *Basic VLSI Design* by Douglas Pucknell and Kamran Eshraghian.
4. *Digital Integrated Circuits* by Jan M. Rabaey.
5. *Semiconductor Physics and Devices* by Donald A. Neamen



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BEC23203T	DIGITAL DESIGN WITH HDL	2L:0T:2P	3 Credits
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Course Outcomes

- Understand the syntax and structure of VHDL and Verilog.
- Design combinational and sequential circuits using HDL.
- Develop FSMs for real-world applications and implement them using HDL.
- Test and verify HDL designs using simulation tools.
- Apply digital design concepts to FPGA-based implementations.

Topics	No of lectures
Module 1: Introduction to Hardware Description Languages (HDL)	8
Overview of HDL : Need for HDLs in digital design, Comparison of VHDL and Verilog, HDL design flow and simulation process.	
VHDL Basics: Structure of a VHDL program: library declarations, entity, and architecture ,Data types, signals, and variables, Concurrent vs. sequential statements	
Verilog Basics:Structure of a Verilog program: module, ports, and instances, Data types: reg and wire, Procedural blocks: always, initial, and continuous assignments	
Tools and Simulation Environments: Introduction to popular tools like ModelSim, Xilinx Vivado, and Synopsys tools	
Module 2: Combinational Circuit Design using HDL	12
Combinational Logic Circuits: Basic gates and Boolean expressions, Multiplexers, decoders, encoders, and demultiplexers, Arithmetic circuits: adders, subtractors, comparators, and ALUs	
Modeling Styles in HDL: Behavioral modeling: procedural blocks, if and case statements, Dataflow modeling: use of operators and continuous assignments, Structural modeling: component instantiation and hierarchical design.	
Hands-on Implementation: Design of combinational circuits using both VHDL and Verilog, Simulation and testing using testbenches.	
<i>Module 3: Sequential Circuit Design using HDL</i>	10
Sequential Circuits Basics: Latches and flip-flops (SR, D, JK, T), Counters: synchronous and asynchronous counters, Registers and shift registers	
Sequential Circuit Modeling in HDL: Modeling flip-flops and latches using procedural blocks, Clock and reset signals in HDL, Design of counters and shift registers	
Timing Considerations: Setup and hold time constraints, Clock skew and its impact on design	
Hands-on Implementation: Design and testing of sequential circuits in HDL	
<i>Module 4: FSM (Finite State Machine) Design using HDL</i>	10
Introduction to FSMs: Types of FSMs: Mealy and Moore machines, State diagrams and state tables	
FSM Design Process: State encoding techniques: binary, one-hot, and gray coding, Implementation of FSMs using HDL , Optimization of FSM design	
Hands-on Implementation: Design of FSMs for real-world applications (e.g., traffic	



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light controller, vending machine, sequence detector), Simulation and verification using testbenches.	
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Recommended Books and Resources

1. *Digital Design* by M. Morris Mano and Michael D. Ciletti.
2. *HDL Programming (VHDL and Verilog)* by Nazeih M. Botros.
3. *Circuit Design with VHDL* by Volnei A. Pedroni.
4. *Digital Design Using Verilog HDL* by Charles Roth, Lizy John, and Byeong Kil Lee.
5. Online tutorials and resources for simulation tools (ModelSim, Vivado).



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BEC23164T	ANALOG AND MIXED-SIGNAL DESIGN	3L:0T:P	3 Credits
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Course Outcomes (CO)

1. Understand the fundamentals of analog circuit design and apply them to solve real-world problems.
2. Analyze and design operational amplifiers for various applications in VLSI.
3. Develop mixed-signal circuits such as data converters, PLLs, and oscillators with performance optimization.
4. Address challenges in noise management, clock synchronization, and co-design of analog and digital blocks.
5. Gain proficiency in using EDA tools for analog and mixed-signal circuit simulation and design.

Topics

No of lectures

Module 1: Fundamentals of Analog Circuits

Introduction to Analog Circuits: Characteristics of analog signals and circuits, Comparison of analog and digital systems, Overview of linear and non-linear circuits

Basic Analog Components: Resistors, capacitors, and inductors in analog circuits, Diodes and transistors: operation and applications, Review of MOSFET models for analog design.

10

Small-Signal Analysis: AC and DC operating points, Small-signal models of MOSFETs, Gain, input/output impedance, and bandwidth calculations

Amplifiers: Single-stage amplifiers: common-source, common-drain, and common-gate configurations, Differential amplifiers: structure, operation, and characteristics, Current mirrors and active loads.

Module 2: Operational Amplifiers in VLSI

Basics of Operational Amplifiers (Op-Amps): Characteristics of ideal and practical op-amps, Parameters: gain, CMRR, PSRR, and slew rate

Op-Amp Architectures: Two-stage op-amp design, Gain-boosted and folded-cascode op-amps, Fully differential op-amps and common-mode feedback.

Applications of Op-Amps: Inverting and non-inverting amplifiers, Integrators, differentiators, and filters (active RC circuits), Comparators and voltage references.

12

Module 3: Module 3: Mixed-Signal Circuits

Introduction to Mixed-Signal Design: Overview of mixed-signal systems, Importance of data converters and signal conditioning, Key challenges in mixed-signal design (noise, mismatch, power supply variations)

Data Converters: Digital-to-Analog Converters (DACs): architectures (binary-weighted, R-2R, current-steering), Analog-to-Digital Converters (ADCs): types (flash, SAR, sigma-delta, pipeline), Performance metrics: resolution, sampling rate, SNR, and ENOB

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Phase-Locked Loops (PLLs) and Oscillators :Basics of PLLs and their applications in clock generation and recovery, Oscillator design: ring oscillators, LC oscillators, and relaxation oscillators.

Module 4: Mixed-Signal Circuits with CO

Clocked Circuits and Timing Considerations: Basics of clock generation and distribution, Clock jitter, skew, and duty-cycle distortion, Design of clock buffers and drivers

Noise in Mixed-Signal Circuits: Sources of noise: thermal, flicker, and quantization noise, Noise-shaping techniques, Strategies to mitigate noise in mixed-signal systems
Case studies: ADC-DAC design in communication systems, Mixed-signal ASICs for sensor interfaces, Co-design techniques for analog and digital blocks

8

Recommended Books and References

1. *Design of Analog CMOS Integrated Circuits* by Behzad Razavi.
2. *CMOS Analog Circuit Design* by Phillip E. Allen and Douglas R. Holberg.
3. *The Design of CMOS Radio-Frequency Integrated Circuits* by Thomas H. Lee.
4. *Mixed-Signal Systems: A Guide to CMOS Circuit Design* by Andrzej Handkiewicz.
5. *Analog and Mixed-Signal Electronics* by Karl Stephan



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BEC23205T	EDA TOOLS FOR VLSI DESIGN	2L:0T:2P	3 CREDITS
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Course Outcomes (CO)

By the end of the course, students will be able to:

1. Understand EDA Tools
2. Simulate Digital Designs
3. Synthesize RTL Designs
4. Analyze Timing
5. Optimize Digital Circuits
6. Integrate Theory with Practice

Topics

No of
lectures

Module 1: Introduction to EDA Tools

Overview of EDA Tools: Importance of EDA in VLSI design and verification, Types of EDA tools: front-end and back-end tools, Key EDA vendors and tools: *Cadence* (Virtuoso, Genus, Innovus) , *Synopsys* (Design Compiler, PrimeTime, IC Compiler), *Mentor Graphics* (QuestaSim, Calibre)

10

Design Flow Using EDA Tools: Specification, RTL Design, Functional Verification, Synthesis, Physical Design, Role of EDA tools at each stage.

Hands-On Practice: Setting up EDA environments and basic navigation in tools like Cadence Virtuoso or Synopsys Design Compiler, Writing simple Verilog/VHDL codes and simulating them using an EDA tool

Module 2: Logic Simulation and Synthesis

Logic Simulation: Role of simulation in the design flow, Behavioral vs. structural simulation, Testbench creation: input stimuli and expected outputs, Debugging designs using waveform analysis tools.

RTL Synthesis: Fundamentals of synthesis: RTL to gate-level netlist, Constraints in synthesis: area, power, and timing constraints, Introduction to standard cells and technology libraries, Handling synthesis reports and interpreting warnings/errors

10

Optimization Techniques: Gate-level optimizations: logic minimization and redundancy removal, Power optimization techniques: clock gating, multi-V_t and power gating.

Hands-On Practice: Writing RTL designs and synthesizing them into gate-level netlists using tools like Synopsys Design Compiler, Comparing pre- and post-synthesis simulation results.

Module 3: Timing Analysis

Introduction to Timing Analysis: Importance of timing analysis in digital design, Setup and hold time concepts, Slack: positive, negative, and zero slack, Propagation delay and critical path analysis

10

Static Timing Analysis (STA): Basics of STA: setup and hold checks, Timing arcs: combinational and sequential delays, Timing exceptions: false paths and multi-cycle



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paths, Crosstalk and its impact on timing

Timing Reports and Optimization: Analyzing STA reports to identify timing violations,
Techniques to fix timing issues: resizing, buffering, and re-synthesis

Hands-On Practice: Performing STA on a synthesized netlist using tools like Synopsys
PrimeTime, Generating and analyzing timing reports

Recommended Books and Resources

1. *ASIC Design with Verilog HDL* by M. Michael D. Ciletti.
2. *Static Timing Analysis for Nanometer Designs* by J. Bhasker and Rakesh Chadha.
3. *Digital Design Using Verilog HDL* by Charles Roth.
4. EDA Tool Documentation: User guides for Cadence, Synopsys, and Mentor Graphics tool

Elective Modules (Choose based on specialization)



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BEC23166T	LOW-POWER VLSI DESIGN	2L:0T:2P	3 CREDITS
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Low-Power VLSI Design

Course Outcomes (CO)

By the end of the course, students will be able to:

- Analyze Power Dissipation in CMOS Circuits
- Apply Power Estimation Techniques
- Implement Low-Power Circuit Techniques
- Design Power-Efficient Architectures
- Explore Advanced Low-Power Technologies
- Integrate Power-Aware Design in Real-World Applications

Topics

No of
lectures

Module 1: Introduction to Power Dissipation in CMOS Circuits

Sources of Power Dissipation: Dynamic power dissipation: capacitive switching, short-circuit power, Static power dissipation: sub threshold leakage, gate leakage, and junction leakage, Other factors affecting power: supply voltage, operating frequency, and temperature.

13

Power-Performance Trade-offs: Relationship between power, delay, and area in VLSI design, Role of scaling (Moore's Law) in power consumption.

Power Estimation Techniques: Analytical estimation of dynamic and static power, Power estimation using EDA tools, Introduction to power-related metrics: power density, power-delay product (PDP), energy-delay product (EDP)

Hands-On Practice: Estimation of power dissipation in a simple CMOS circuit using SPICE simulation, Analysis of power components in an inverter chain.

Module 2: Low-Power Design Techniques

Techniques at the Circuit Level: Voltage scaling: static and dynamic voltage scaling (DVS), Use of multi-threshold CMOS (MTCMOS), Power gating techniques: sleep transistors and retention registers, Clock gating to reduce switching power

Techniques at the Architecture Level: Parallelism and pipelining for power optimization, Dynamic voltage and frequency scaling (DVFS), Low-power SRAM design: reducing bitline swing, banking, and leakage control

12

Algorithmic and System-Level Techniques: Power-aware algorithm design, Energy-efficient data encoding schemes, Operating system-level power management strategies

Low-Power Design in Digital Circuits: Optimization of combinational and sequential circuits for power efficiency, Techniques for low-power flip-flops and latches

Hands-On Practice: Implementation of power reduction techniques in combinational and sequential circuits using SPICE and Verilog. Simulation and comparison of power in gated vs. ungated clock circuits.



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Module 3: Advanced Topics

Low-Power Applications: Power-efficient designs in mobile and IoT devices, Challenges in low-power VLSI for AI and machine learning accelerators.

Emerging Technologies for Low Power: FinFETs and their role in reducing leakage power, Advanced low-power techniques in beyond-CMOS technologies

Power-Aware EDA Tools: Introduction to power analysis tools like Synopsys PrimePower and Cadence Voltus , Power optimization in synthesis and place-and-route flows

Analysis of low-power processors (e.g., ARM Cortex-M series), Power optimization in FPGA-based designs

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Recommended Books and Resources

1. *Low-Power CMOS VLSI Circuit Design* by Kaushik Roy and Sharat Prasad.
2. *Digital Integrated Circuits: A Design Perspective* by Jan M. Rabaey.
3. *Practical Low Power Digital VLSI Design* by Gary K. Yeap.
4. *Low Power Design Methodologies* by Jan Rabaey and Massoud Pedram.
5. EDA Tool Documentation: Power analysis tools like Synopsys PrimeTime-PX, Cadence Voltus.



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BEC23166T	SYSTEM-ON-CHIP (SOC) DESIGN	2L:0T:2P	3 CREDITS
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- Understand SoC Design Principles
- Integrate IPs into SoC Designs
- Verify SoC Designs
- Address Advanced SoC Challenges
- Utilize EDA Tools for SoC Design
- Bridge Theory and Practice

Topics

No of
lectures

Module 1: Introduction to SoC Design Principles

Overview of SoC: Evolution of SoC: From single-chip systems to heterogeneous SoCs, Importance and applications of SoC in consumer electronics, IoT, automotive, and AI

Architecture of SoC: Components of an SoC: processors, memory subsystems, peripherals, and interconnects, Processor types: general-purpose processors (GPP), digital signal processors (DSP), application-specific instruction-set processors (ASIP)

Design Challenges: Power, performance, and area (PPA) trade-offs, Scalability, manufacturability, and reliability challenges

Hands-On Practice: Analyze the architectural block diagram of a simple SoC and identify its components, Create a basic SoC design specification.

10

Module 2: IP Integration

Introduction to IP Cores: Types of IP cores: soft IP, firm IP, and hard IP, Standard IP interfaces and protocols: AXI, AHB, APB (AMBA protocols)

IP Selection and Customization: Criteria for IP selection: performance, compatibility, licensing, and reuse, Integration of custom and third-party IP into SoC designs

Memory Design in SoC: Types of memory: on-chip SRAM, DRAM, non-volatile memory (NVM), Memory hierarchy in SoC for performance optimization

Interconnect Design: Interconnect architectures: bus-based vs. network-on-chip (NoC), Address decoding, arbitration, and clock domain crossing (CDC) issues

Hands-On Practice: Integrate a soft IP (e.g., UART or GPIO) into an SoC framework using Verilog or VHDL. Simulate the functionality of an SoC design with multiple IPs.

12

Module 3: Verification of SoC Designs

Verification Methodologies: Need for verification in SoC design, Overview of simulation-based, formal, and emulation-based verification

Testbench Development: Writing testbenches for IPs and subsystems, Functional and constrained-random testing

System-Level Verification : SoC verification using hardware-software co-simulation, Protocol checking for AMBA interfaces

Debugging and Coverage: Debugging SoC designs using waveforms and logs, Code and functional coverage analysis

Hands-On Practice: Develop a verification testbench for an IP using UVM (Universal Verification Methodology), Perform system-level simulation of an SoC with integrated

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IPs.

Module 4: Advanced Topics in SoC Design

Low-Power SoC Design: Techniques for power management: DVFS, clock gating, and power gating, Designing with power-aware tools

Security in SoC: Security challenges in SoC design, Hardware-based security features (secure boot, encryption engines)

SoC Prototyping and Validation: Prototyping using FPGAs, Post-silicon validation techniques

Hands-On Practice: Implement a basic SoC on an FPGA platform, Perform power analysis of an SoC design.

8

Recommended Books and Resources

6. *Low-Power CMOS VLSI Circuit Design* by Kaushik Roy and Sharat Prasad.
7. *Digital Integrated Circuits: A Design Perspective* by Jan M. Rabaey.
8. *Practical Low Power Digital VLSI Design* by Gary K. Yeap.
9. *Low Power Design Methodologies* by Jan Rabaey and Massoud Pedram.
10. EDA Tool Documentation: Power analysis tools like Synopsys PrimeTime-PX, Cadence Voltus.



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BEC23166T	PHYSICAL DESIGN AND VERIFICATION	2L:0T:2P	3 CREDITS
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Course Objectives (COs):

By the end of the course, students will be able to:

1. **CO1:** Understand the principles and stages of physical design in VLSI circuits.
2. **CO2:** Perform floorplanning, placement, and routing of standard cell-based designs.
3. **CO3:** Apply Design Rule Checks (DRC) to ensure manufacturability and adherence to fabrication rules.
4. **CO4:** Use Layout Versus Schematic (LVS) checks to verify the correctness of the layout and its correspondence with the original schematic design.
5. **CO5:** Analyze and solve common problems encountered during physical design and verification stages in modern VLSI systems.

Detailed Syllabus:

Topics

No of
lectures

Unit 1: Introduction to Physical Design

Overview of VLSI Design Flow: Front-end vs. back-end design, Role of physical design in the VLSI design flow

6

Basic Concepts in Physical Design: Transistor-level and gate-level layouts, CMOS process technology overview, Design constraints and specifications in physical design

Unit 2: Floorplanning

Floorplanning Basics: Purpose of floorplanning in physical design, Area estimation and optimization, Design constraints: aspect ratio, pin placement, and power grid planning

8

Block-level Floorplanning: Partitioning techniques, Power distribution network (PDN) planning, Placement of macros, IP blocks, and core logic cells

Tools for Floorplanning: Introduction to EDA tools (e.g., Cadence, Synopsys, Mentor Graphics)

Unit 3: Placement

Placement Overview: Importance of placement in physical design, Types of placement: global vs. detailed placement

10

Placement Algorithms: Simulated annealing, Force-directed algorithms, Timing-driven placement, Congestion-aware placement

Placement Optimization: Wire length minimization, Power and performance trade-offs.

Unit 4: Routing

Routing Basics: Types of routing: global routing, detailed routing, Routing layers and via management

8

Routing Algorithms: Maze routing, Steiner tree routing, Timing-driven and congestion-aware routing, Multi-layer routing considerations

Routing Optimization: Optimization of wire length, delay, and power consumption, Crosstalk and noise considerations



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Unit 5: Design Rule Check (DRC)

Introduction to DRC: What is Design Rule Checking?, Importance of DRC in physical design and manufacturability

DRC Constraints: Minimum spacing, width, and enclosure constraints, Via rules and layer-specific design constraints

Automated DRC Tools: Working with DRC in EDA tools (e.g., Cadence Virtuoso, Mentor Graphics Calibre)

6

Unit 6: Layout vs. Schematic Check (LVS)

Introduction to LVS: What is LVS and why it is necessary in verification?, LVS tools and their role in ensuring design correctness

LVS Methodology: Comparing layout with the schematic to ensure electrical integrity, Identifying common layout errors (shorts, opens, mismatches)

LVS Debugging: Resolving LVS violations and mismatch errors, Handling device modeling and parasitics during LVS

6

Unit 7: Physical Design Challenges and Solutions

Challenges in Physical Design: Timing closure issues, Power and noise management, Crosstalk and signal integrity

Advanced Topics in Physical Design: Multi-patterning and its impact on routing, Design for manufacturability (DFM), 3D IC design and through-silicon vias (TSVs)

7

Unit 8: Physical Design Tools and Flow

Overview of Physical Design Tools: Cadence, Synopsys, and Mentor Graphics tools for physical design, Integration of physical design with other design phases

4

Recommended Textbooks:

1. "VLSI Physical Design: From Graph Partitioning to Timing Closure" by Andrew B. Kahng, Igor L. Markov, et al.
2. "CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H. E. Weste and David Harris
3. "Digital Integrated Circuits: A Design Perspective" by Jan M. Rabaey



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

BEC23207T	PHYSICAL DESIGN AND VERIFICATION	2L:0T:2P	3 CREDITS
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VLSI Testing and Verification

Course Objectives

By the end of the course, students will be able to:

1. **CO1:** Understand the importance of testing and verification in the VLSI design process.
2. **CO2:** Apply fault modeling and test pattern generation techniques to identify and isolate faults in digital circuits.
3. **CO3:** Design circuits with testability features using design-for-testability (DFT) techniques.
4. **CO4:** Use simulation-based and formal verification methods to ensure functional correctness of VLSI designs.
5. **CO5:** Analyze test coverage and optimize testing processes for time and cost efficiency.
6. **CO6:** Work with industry-standard testing and verification tools for real-world applications.

Topics

No of lectures

Unit 1: Introduction to VLSI Testing

Role of Testing in VLSI Design: Ensuring quality and reliability in IC manufacturing.
Testing Challenges in Modern VLSI Circuits: Complexity, high transistor count, and miniaturization.

6

Basic Terminologies: Faults, errors, and failures, Yield and defect levels.

Unit 2: Fault Modeling and

Types of Faults in VLSI Circuits: Stuck-at faults, bridging faults, delay faults, and transient faults.

8

Fault Models: Single stuck-at fault model, Path delay and transition fault models.

Fault Simulation: Algorithms for fault simulation: parallel, deductive, and concurrent, Tools for fault simulation.

Unit 3: Test Pattern Generation

Automatic Test Pattern Generation (ATPG): Introduction to ATPG, Algorithms for ATPG: D-algorithm, PODEM, FAN, etc.

8

Test Metrics: Fault coverage, test efficiency, and computational complexity.

Built-in Self-Test (BIST): Architecture and advantages of BIST. Test pattern generation and response analysis in BIST.

Unit 4: Design-for-Testability (DFT) Techniques

Importance of DFT: Improving testability during design.

8

Scan-Based Testing: Scan design principles. Full-scan and partial-scan techniques.



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Boundary Scan Testing (IEEE 1149.1): JTAG architecture and operation.

Memory Testing: March tests, checkerboard tests, and fault models for SRAM/DRAM

Unit 5: Logic Verification

Concept of Logic Verification : Differences between simulation and verification. **6**

Functional Verification: Techniques and tools (e.g., UVM, SystemVerilog).

Simulation-Based Verification: Testbench design and coverage analysis.

Unit 6: Formal Verification

Overview of Formal Verification: Equivalence checking, model checking, and property checking. **8**

Static Timing Analysis (STA): Importance of STA in VLSI verification, Timing constraints, setup/hold time, and slack analysis.

Advanced Verification Techniques: Assertion-based verification (ABV), Verification methodologies: VMM, OVM, and UVM.

Unit 7: Test Compression and Test Optimization

Test Data Compression: Reducing test data volume, Methods for test compression

Power-Aware Testing: Challenges of testing low-power designs, Techniques to minimize power during testing. **6**

Economic Aspects of Testing: Cost vs. coverage trade-offs.

Unit 8: Testing Tools and Case Studies

*Overview of Testing Tools: Tools from Cadence, Synopsys, and Mentor Graphics for ATPG, BIST, and DFT. Real-world examples of testing and verification challenges in IC design. **6***

Recommended Textbooks:

1. **"Digital Systems Testing and Testable Design"** by Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman.
2. **"VLSI Test Principles and Architectures"** by Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen.
3. **"CMOS VLSI Design: A Circuits and Systems Perspective"** by Neil H. E. Weste and David Harris.